What is claimed is:

Sub A1

1. A processor, comprising:

a processor core;

a data memory accessed by said processor core; and

an extended arithmetic unit, connected to an exterior of said processor core, for processing a particular instruction,

said extended arithmetic unit executing an arithmetic operation by using arithmetic operation data retained in a register file in said processor core, and outputting a result of an arithmetic operation directly to said processor core,

said processor core saving the result of the arithmetic operation executed by said extended arithmetic unit and inputted therefrom in said register file in said processor core.

2. A processor, comprising:

a processor core;

a data memory accessed by said processor core; and

an extended arithmetic unit, connected to an exterior of said processor core, for processing a particular instruction,

said processor core, at least including:

an instruction memory for storing an instruction to be executed;

an instruction decode unit for reading out an instruction from said instruction memory to decode the instruction, in case that the instruction decoded is an extended arithmetic unit control instruction that should be executed by said extended arithmetic unit connected to the exterior of said processor core, said instruction decode unit also outputting at least an instruction code of said extended arithmetic unit control instruction to said extended arithmetic unit;

a register file for retaining arithmetic operation data of an arithmetic operation that should be executed by the

instruction decoded, in case that said arithmetic operation data is data of said extended arithmetic unit control instruction, said register file also outputting said arithmetic operation data to said extended arithmetic unit;

a first operational section for executing the instruction decoded; and

an extended arithmetic unit, at least including,

a second operational section for executing an arithmetic operation specified by said extended arithmetic unit control instruction by using said arithmetic operation data retained in said register, and outputting an execution result of the arithmetic operation to said processor core.

3. The processor according to claim 1, wherein,

in case that the instruction decoded is said extended arithmetic unit control instruction, said processor core outputs to said extended arithmetic unit at least an instruction code that specifies an action involved in an arithmetic operation in said extended arithmetic unit and an instruction valid signal that indicates said instruction code is valid.

4. The processor according to claim 1, wherein said arithmetic operation data outputted to said extended arithmetic unit is a value read out from said register file in said processor core in accordance with a register number specified by a part of said extended arithmetic unit control instruction.

5. The processor according to claim 1, wherein said processor core includes a pipeline control unit for controlling pipeline processing in an interior of said processor core and in said extended arithmetic unit.

6. The processor according to claim 5, wherein said pipeline control unit outputs to said extended arithmetic unit a first pipeline stop signal for suspending execution of an instruction

in said extended arithmetic unit.

7. The processor according to claim 5, wherein said pipeline control unit outputs to said extended arithmetic unit a pipeline flush signal for abandoning execution of an instruction outputted to said extended arithmetic unit.

8. The processor according to claim 5, wherein said pipeline control unit stops execution of an instruction in said processor core in accordance with a second pipeline stop signal for suspending execution of an instruction inputted from said extended arithmetic unit and executed by said processor core.

9. The processor according to claim 1, wherein said extended arithmetic unit outputs to said processor core an arithmetic operation result invalidating signal that invalidates an execution result of an arithmetic operation executed in said processor core.

10. The processor according to claim 1, wherein said data memory:

receives from said extended arithmetic unit at least one of an address for memory access, data, a write control signal for controlling data writing, and a read control signal for controlling data reading;

reads out the data from a region specified by said address and outputs the data to said extended arithmetic unit in case that data reading is carried out because said read control signal is asserted; and

writes the data inputted from said extended arithmetic unit into a region specified by said address in case that data writing is carried out because said write control signal is asserted.

11. The processor according to claim 1, wherein said extended arithmetic unit includes:

a plurality of arithmetic circuits;

a first pipeline register for storing a processing result by an arithmetic circuit in a preceding stage at a rising of a following clock; and

a second pipeline register for storing a processing result by an arithmetic circuit in a succeeding stage at the rising of the following clock.

12. A processor core connected to an extended arithmetic unit for processing a particular instruction to an exterior thereof, comprising:

an instruction memory for storing an instruction to be executed;

an instruction decode unit for reading out an instruction from said instruction memory to decode the instruction, in case that the instruction decoded is an extended arithmetic unit control instruction that should be executed by said extended arithmetic unit connected to the exterior of said processor core, said instruction decode unit also outputting at least an instruction code of said extended arithmetic unit control instruction to said extended arithmetic unit; and

a register file for retaining arithmetic operation data of an arithmetic operation that should be executed by the instruction decoded, and in case that said arithmetic operation data is data for said extended arithmetic unit control instruction, said register file also outputting said arithmetic operation data to said extended arithmetic unit and storing a result of an arithmetic operation executed in said extended arithmetic unit.

13. The processor core according to claim 12, wherein, in case that the instruction decoded is said extended arithmetic unit control instruction, said instruction decode unit outputs to said extended arithmetic unit at least an instruction code that specifies an action involved in an arithmetic operation by said extended arithmetic unit and an instruction valid

signal that indicates said instruction code is valid.

14. The processor core according to claim 12, wherein said arithmetic operation data outputted to said extended arithmetic unit is a value read out from said register file in said processor core in accordance with a register number specified by a part of said extended arithmetic unit control instruction.

15. The processor core according to claim 12, further comprising a pipeline control unit for controlling pipeline processing in an internal of said processor core and in said extended arithmetic unit.

16. The processor core according to claim 15, wherein said pipeline control unit outputs to said extended arithmetic unit a first pipeline stop signal for suspending execution of an instruction in said extended arithmetic unit.

17. The processor core according to claim 15, wherein said pipeline control unit outputs to said extended arithmetic unit a pipeline flush signal for abandoning execution of an instruction outputted to said extended arithmetic unit.

18. The processor core according to claim 15, wherein said pipeline control unit stops execution of an instruction in said processor core in accordance with a second pipeline stop signal, inputted from said extended arithmetic unit, for suspending execution of an instruction in said processor core.

19. The processor core according to claim 15, wherein said pipeline control unit receives from said extended arithmetic unit an arithmetic operation result invalidating signal that invalidates an execution result of an arithmetic operation in said processor core, and invalidates the execution result of the arithmetic operation in said processor core.

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